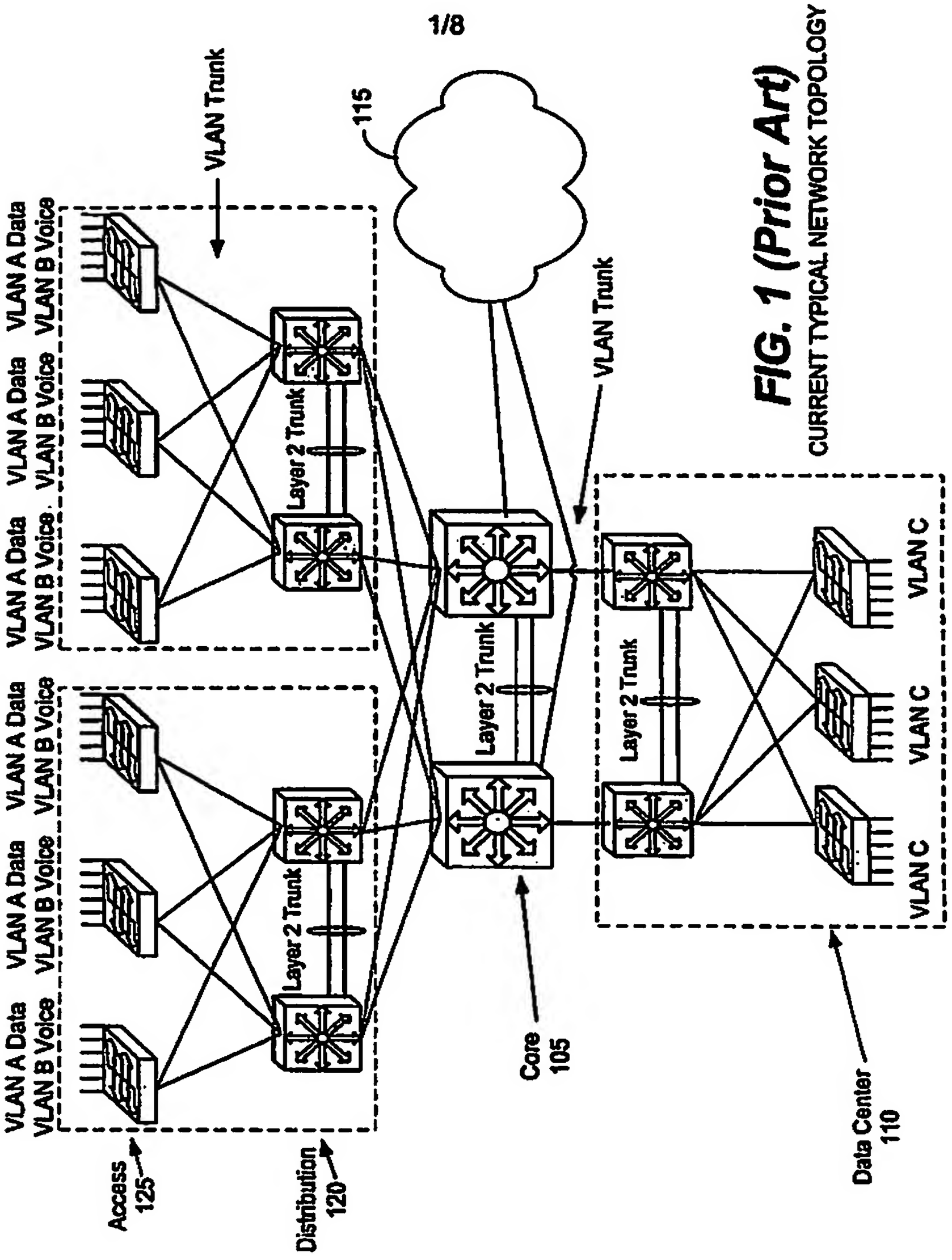

FIG. 1 (Prior Art)
CURRENT TYPICAL NETWORK TOPOLOGY

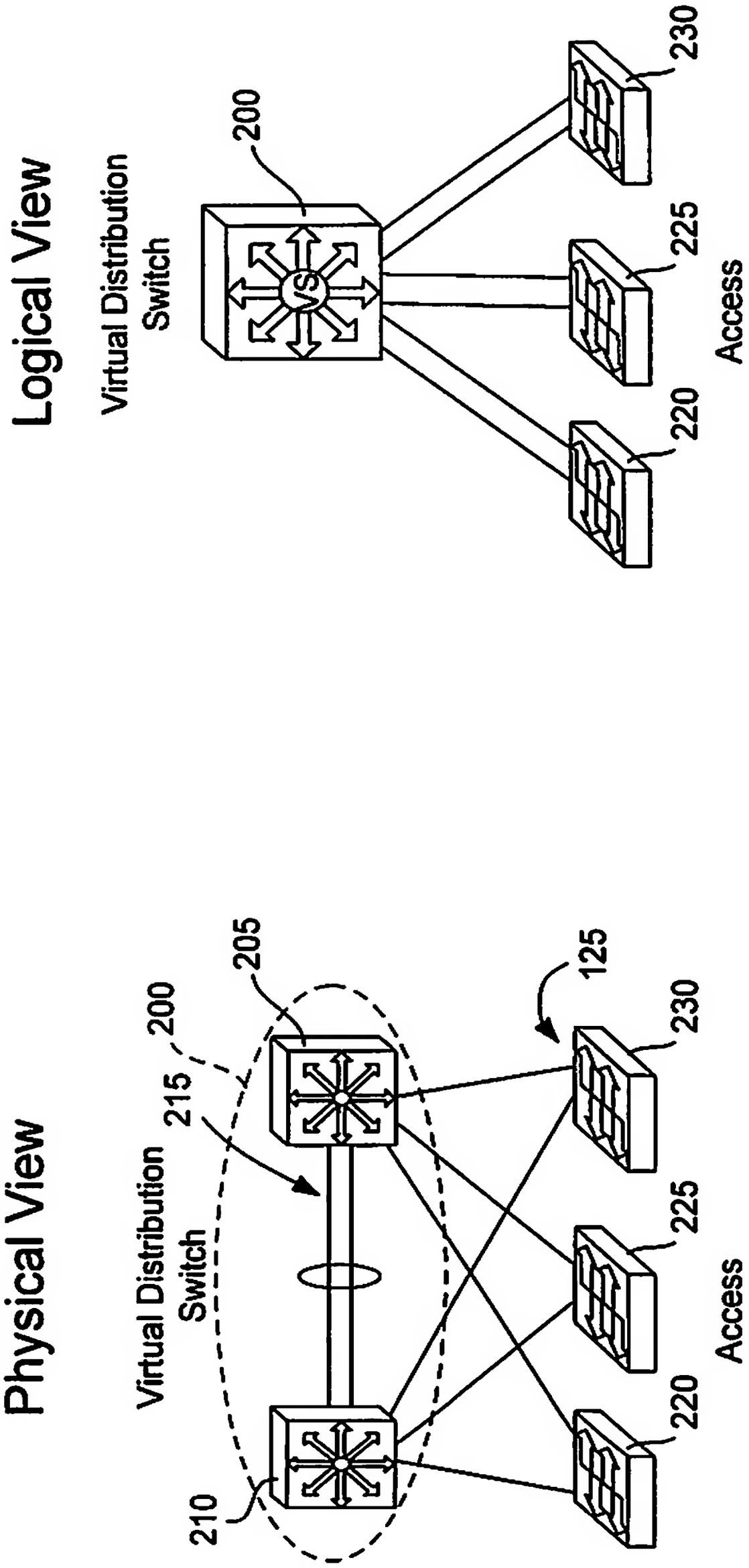
Logical View
Virtual Distribution Switch
200
230
225
220
Access

FIG. 2B

Physical View
200
205
215
125
230
Virtual Distribution Switch
225
220
210
Access

FIG. 2A

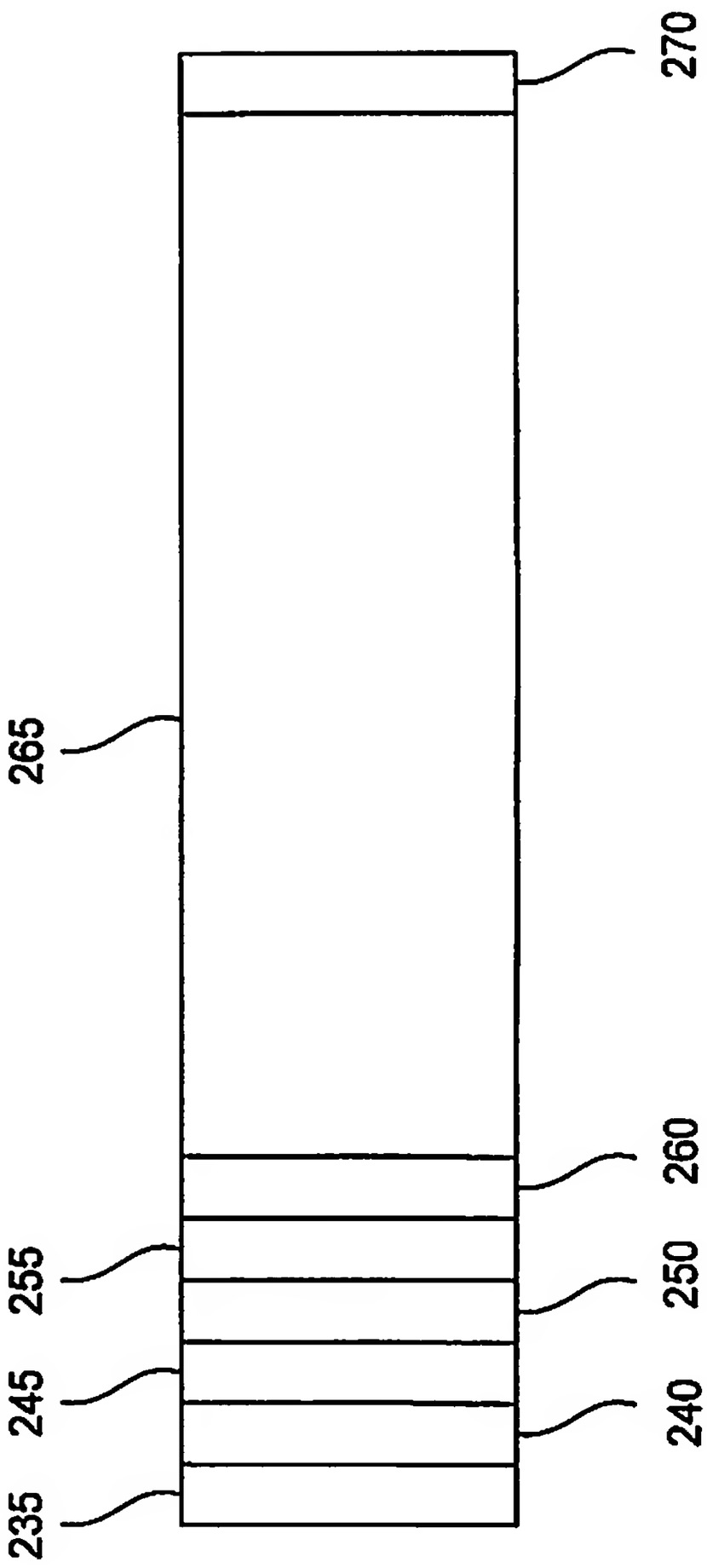

FIG. 2C

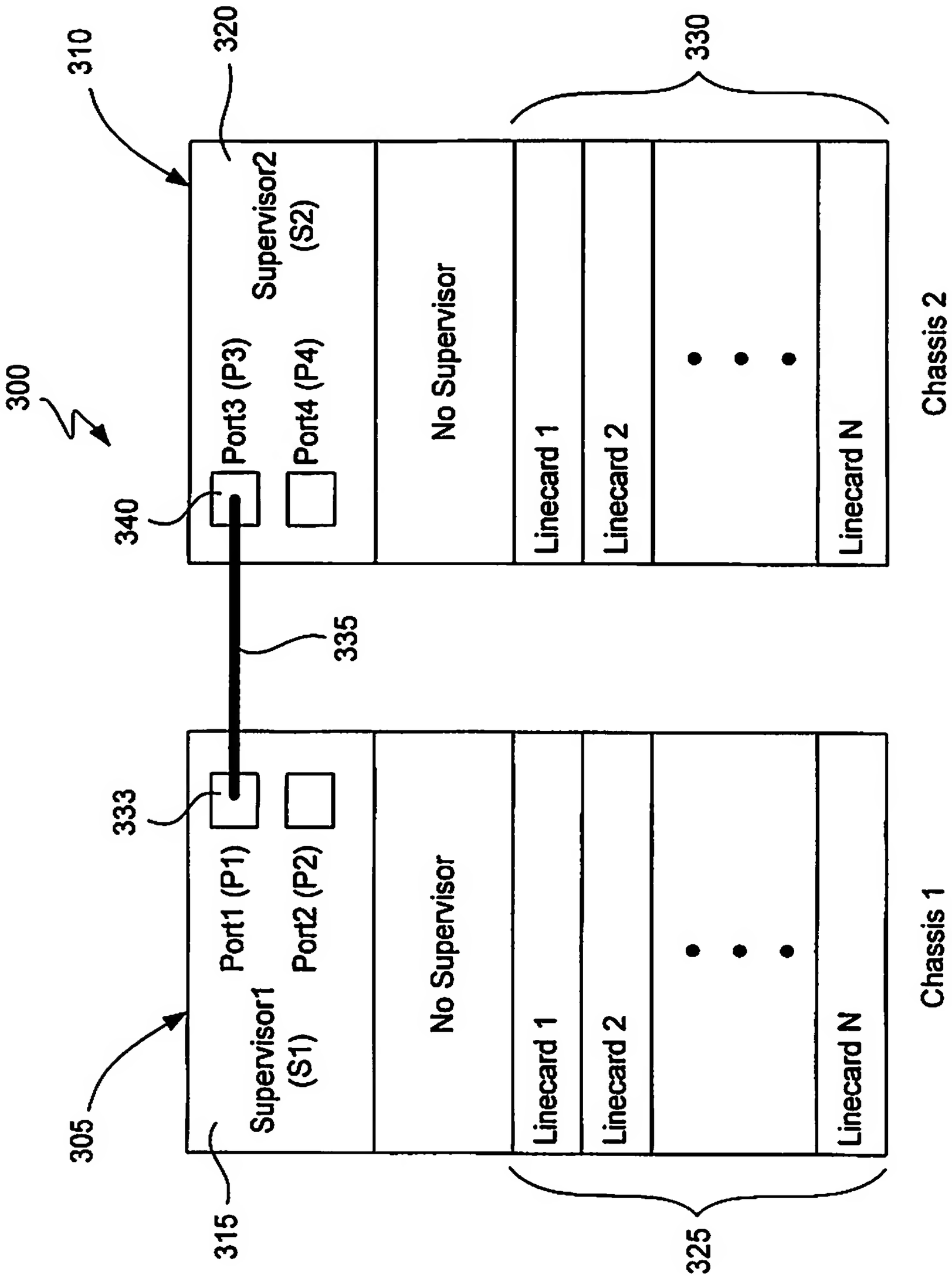
310
320
330
300
340
335
333
305
315
325
Supervisor2 (S2)
Port3 (P3)
Port4 (P4)
No Supervisor
Linecard 1
Linecard 2
Linecard N
Chassis 2
Supervisor1 (S1)
Port1 (P1)
Port2 (P2)
No Supervisor
Linecard 1
Linecard 2
Linecard N
Chassis 1

FIG. 3

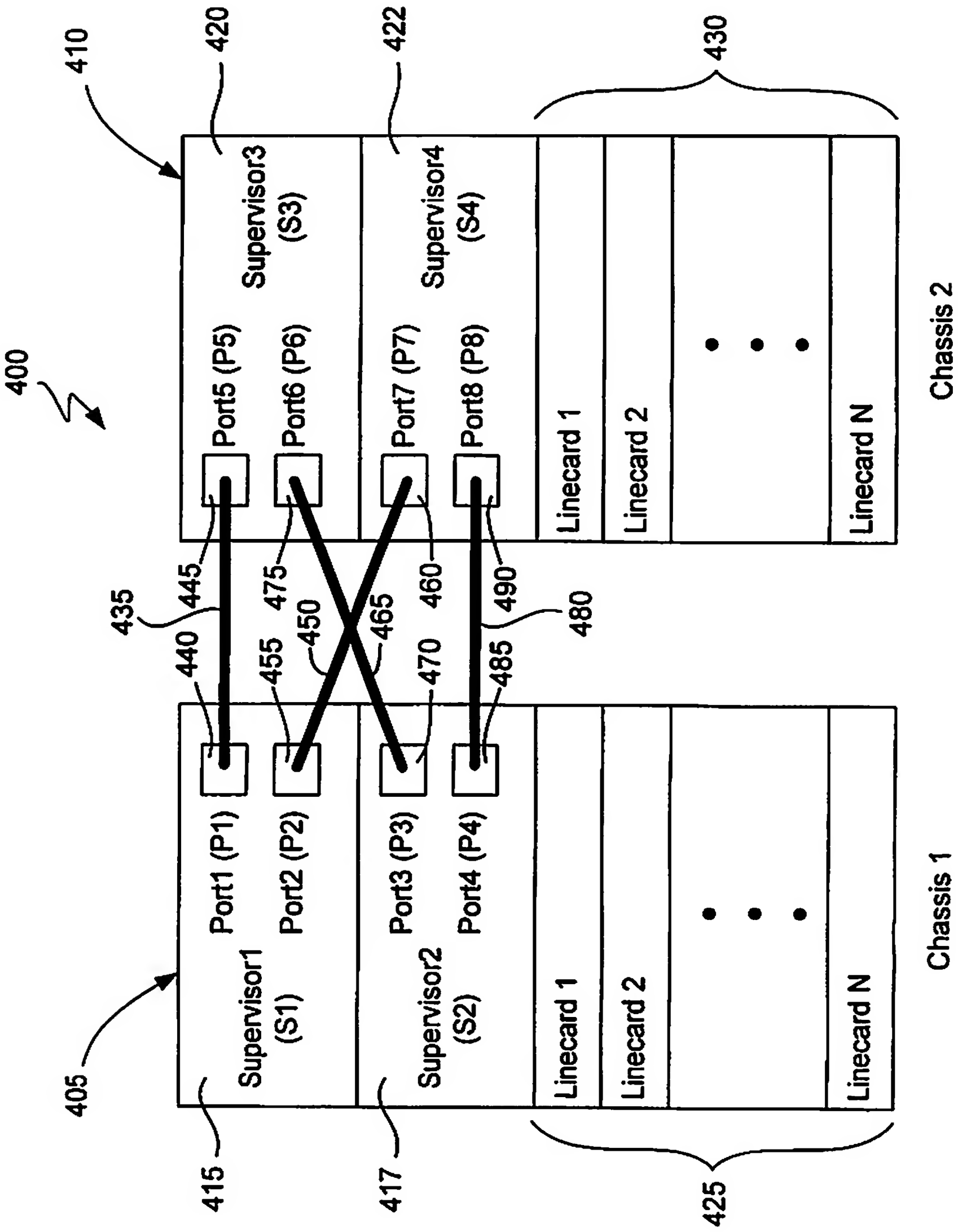
400
405
410
415
417
420
422
425
430
435
440
445
450
455
460
465
470
475
480
485
490
Supervisor1 (S1)
Supervisor2 (S2)
Supervisor3 (S3)
Supervisor4 (S4)
Port1 (P1)
Port2 (P2)
Port3 (P3)
Port4 (P4)
Port5 (P5)
Port6 (P6)
Port7 (P7)
Port8 (P8)
Linecard 1
Linecard 2
Linecard N
Chassis 1
Chassis 2

FIG. 4

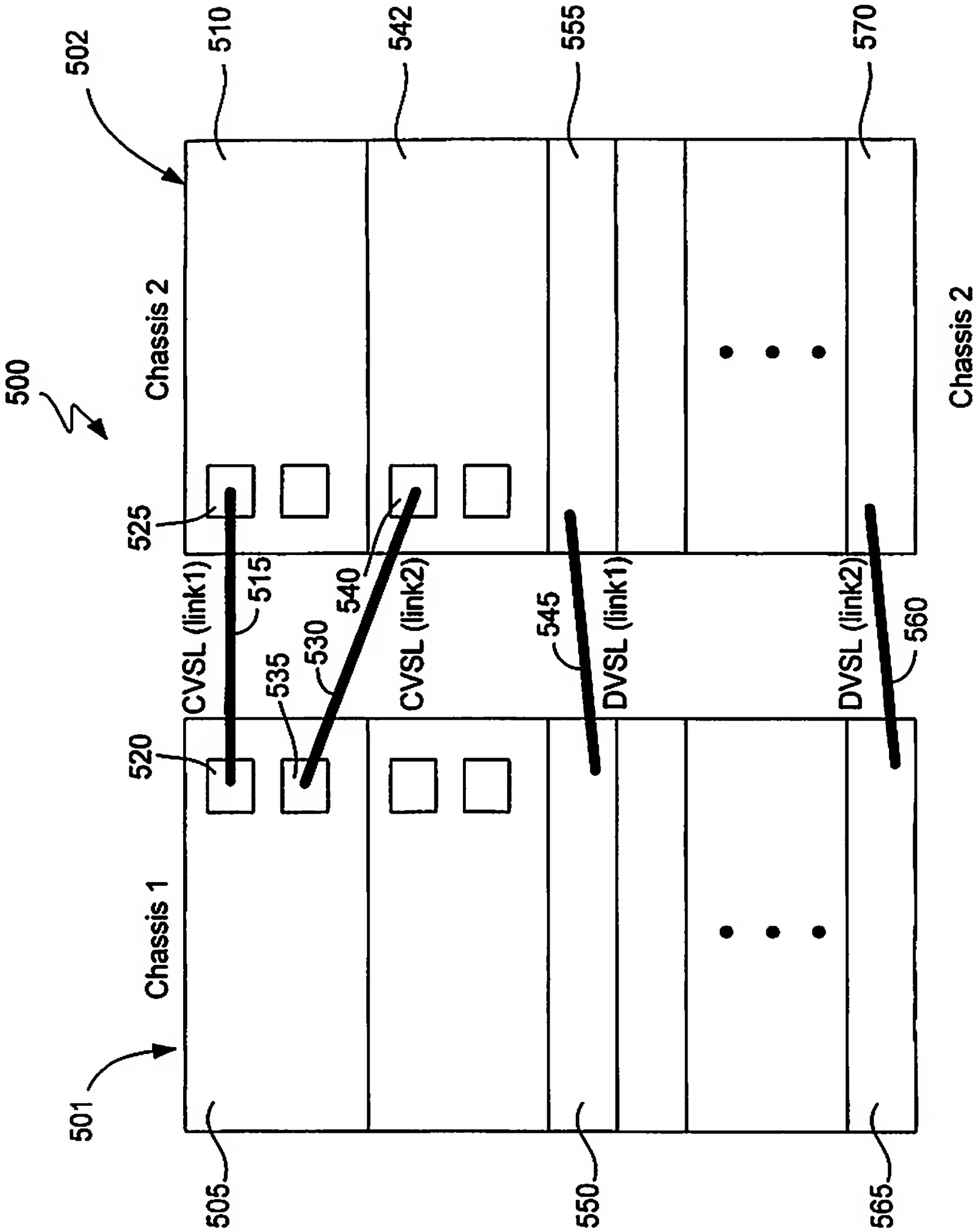
500
501
502
510
542
555
570
Chassis 2
Chassis 2
Chassis 1
525
520
505
550
565
515
535
530
540
545
560
CVSL (link1)
CVSL (link2)
DVSL (link1)
DVSL (link2)

FIG. 5

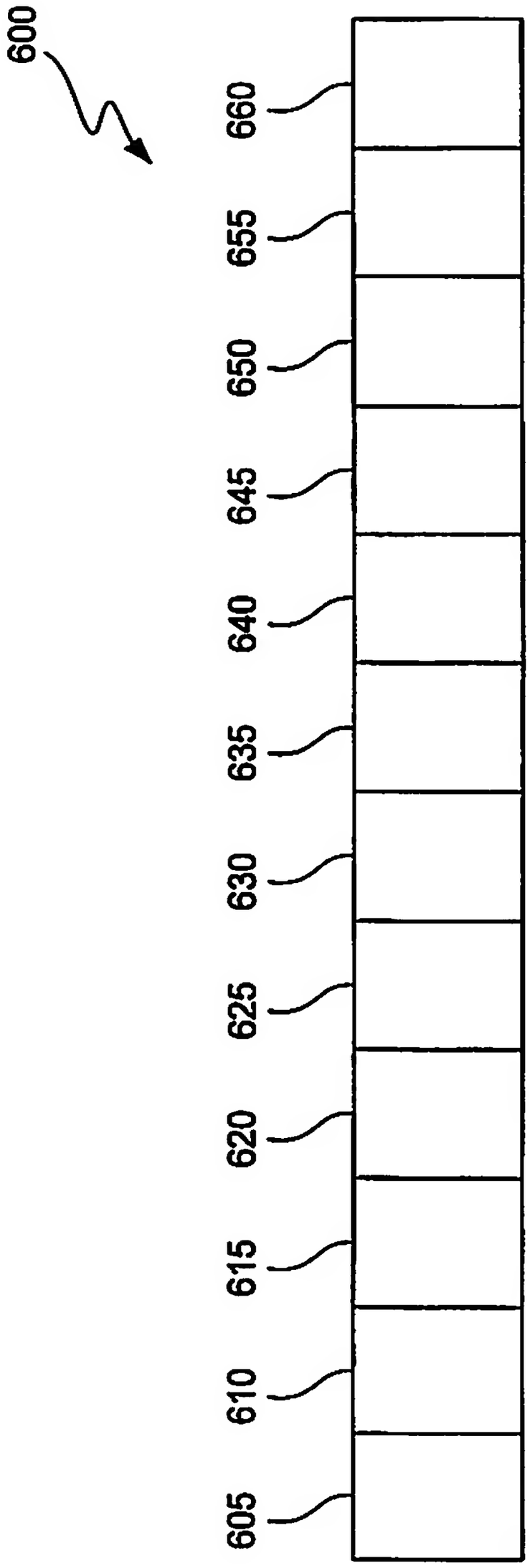

FIG. 6

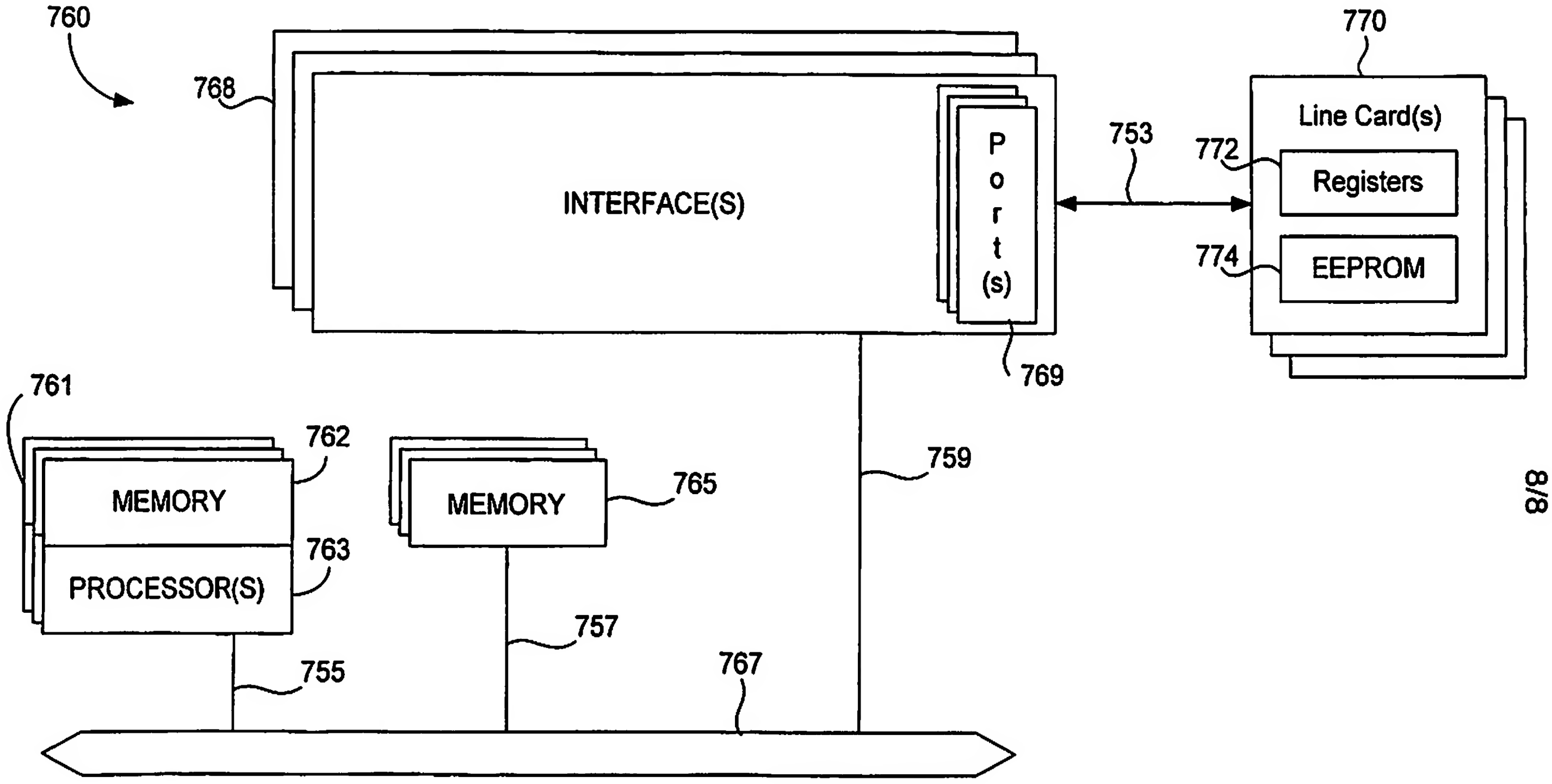
760
768
INTERFACE(S)
P
o
r
t
(s)
769
753
770
Line Card(s)
772
Registers
774
EEPROM
761
762
MEMORY
763
PROCESSOR(S)
765
MEMORY
759
757
755
767

FIG. 7